REMARKS

The application has been amended to place the application in condition for allowance at the time of the next Official Action.

Claims 1, 3-8, 24 and 26-30 were previously pending in the application. Claim 4 is canceled and new claims 31-34 are added. Therefore, claims 1, 3, 5-8 and 26-34 are presented for consideration.

Claims 1, 3-8, 24 and 26-30 were rejected as unpatentable over SHEU et al. 6,694,208 in view of applicants' disclosed prior art. That rejection is respectfully traversed.

Claim 1 is amended and recites forming a plurality of electrode test pads on an uppermost surface of a first metal wiring layer for carrying out a provisional yield rate test. Claim 1 also recites subjecting the wafer to a provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on the wafer is acceptable or unacceptable.

The Official Action offers column 1, lines 20-25 and column 2, lines 57-65 of the SHEU reference as disclosing subjecting the wafer to a provisional yield-rate test.

However, this characterization of SHEU is neither consistent with the disclosure of SHEU, nor meets the recited limitations.

Column 1, lines 20-25 of SHEU disclose that to improve yield rate, test structure or test circuitry, is formed alongside

the chips to allow electrical tests to be conducted during and after manufacturing.

SHEU neither discloses forming a plurality of electrode test pads on a first metal wiring layer (of the chip area) for carrying out a provisional yield rate test as recited, nor discloses that the test pads are on an uppermost surface of the first metal wiring layer.

Rather, as set forth above, the test circuitry is formed alongside the chip area.

Moreover, the test circuitry of SHEU is used to test a finished wafer. SHEU does not disclose a provisional yield rate test on a semi-finished wafer.

Column 2, lines 1-39 of SHEU disclose that a predetermined number of wafers are processed. The processed or completed wafers are then examined. When defects occur, adjustments are made to the process or equipment so that the detected defect will be minimized or eliminated on subsequent wafers.

Accordingly, the yield rate test of SHEU determines how further processing will proceed on the next batch of wafers. SHEU does not disclose performing a provisional yield rate test on a wafer and then further processing that same wafer.

Thus, SHEU nether discloses a plurality of electrode pads on an uppermost surface of first metal wiring layer, not that

those pads are for performing a provisional yield rate test on semi-finished wafers.

Applicants' disclosed prior art does not overcome the shortcomings of SHEU. Rather, as set forth on page 35, line 29 to page 36, line 4 in describing applicants' prior art Figure 17, a plurality of electrode pads are only on the second layer of the finished device.

As SHEU uses a test circuit alongside the chips to adjust processing on subsequent wafers and as applicants' disclosed prior art only has test pads on a second wiring layer, performing a provisional yield-rate test on a plurality of electrode pads on an uppermost surface of a first wiring layer would not have been obvious to one having ordinary skill in the art.

Accordingly, for the reasons set forth above, claim 1 is believed patentable over the proposed combination of references.

Claims 3 and 5-8 depend from claim 1 and further define the invention and are also believed patentable at least for depending from an allowable independent claim.

Independent claim 24 recites performing a provisional yield-rate test to determine whether each first metal wiring layer is acceptable or unacceptable. The first metal wiring layer has a plurality of electrode pads formed on an uppermost surface thereof, for carrying out the provisional yield-rate test.

The analysis above regarding claim 1 is equally applicable to claim 24.

Claims 26-28 depend from claim 24 and further define the invention and are also believed patentable at least for depending from an allowable independent claim.

Independent claim 29 recites a first metal wiring layer having a first test section and performing a provisional yield-rate test using the first test section. Claim 29 also recites further processing the wafer to form a second metal wiring layer.

As set forth above, column 1, lines 21-24 of SHEU disclose test circuitry formed alongside the chip. SHEU does not disclose a test section on a first wiring layer of the chip.

In addition, the wafer of SHEU is a processed as a finished product, SHEU does not continue processing the same wafer to form a second wiring layer as suggested in the Official Action. Rather, as set forth above, SHEU adjusts his process for subsequent wafers.

Independent claim 30 recites processing a wafer by at least one of depositing and patterning to form a second metal wiring layer based on the results of the testing on the first metal wire layer.

The proposed combination of references does not disclose this feature. Rather, SHEU discloses adjusting a process for subsequent wafers based on the results of a completely finished wafer, and the Applicant's disclosed prior art only teaches

testing a second wiring layer and does not disclose testing a first wiring layer.

As each of the limitations is not disclosed by the combination of references, their combination would not have been sufficient to render the claims *prima facie* obvious.

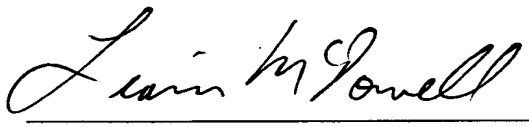
New claims 31-34 are added. Support for the new claims can be found in Figure 5 and the original claims.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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